What is claimed is:

1. A liquid crystal driving semiconductor chip comprising:

a control section which stores display data into a memory section in accordance with an operation control signal;

a drive section which drives a liquid crystal display in accordance with said display data stored in said memory section;

a power-supply electrode to which power is supplied from an external power supply circuit;

a monitor electrode which is supplied with a power supply potential of said power supply circuit in a path different from a path for said power supplied from said power supply circuit;

a control electrode to be supplied with a control signal to enable an operation of said control section;

a CMOS inverter which detects a logical level of said control signal to be supplied to said control electrode; and

a level monitor section which has an MOS transistor for detecting a logical level of said power supply potential to be supplied to said monitor electrode, outputs a detection signal from said CMOS inverter to said control section as said operation control signal when said MOS transistor detects a correct logical level, and stops outputting said operation control signal when said MOS

transistor does not detect the correct logical level.

2. The liquid crystal driving semiconductor chip according to claim 1, wherein said power supply potential to be supplied to said monitor electrode is a positive potential and said MOS transistor is an N type transistor.

3. The liquid crystal driving semiconductor chip according to claim 1, wherein said power supply potential to be supplied to said monitor electrode is a negative potential and said MOS transistor is a P type transistor.

4. A liquid crystal driving semiconductor chip comprising:

a control section which stores display data into a memory section in accordance with an operation control signal;

a drive section which drives a liquid crystal display in accordance with said display data stored in said memory section;

a first control electrode to be supplied with a first control signal to enable an operation of said control section;

a second control electrode to be supplied with a second control signal which is said first control signal whose logical level is inverted;

a first CMOS inverter which detects a logical level of said first control signal to be supplied to said first control electrode; and

a level monitor section which has a second CMOS

inverter which detects a logical level of said second control signal to be supplied to said second control electrode, outputs a detection signal from said first CMOS inverter to said control section as said operation control signal when a logical level of a signal obtained by inverting a detection signal from said first CMOS inverter coincides with a logical level of a detection signal from said second CMOS inverter, and stops outputting said operation control signal when said logical levels do not match with each other.